Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A demodulation apparatus for a communication system, comprising:

an analog-to-digital converter device to convert an intermediate frequency signal into a digital signal and provide a quadrature component and an in-phase component of the digital signal;

a plurality of filters to filter components of the digital signal outputted from the analog-to-digital converter device in a low pass band respectively; and

a CDMA modem to demodulate outputs of the plurality of filters,

wherein the analog-to-digital converter device includes:

a quantizer to convert the intermediate frequency signal into the digital signal;

a latch circuit to receive the digital signal and output first and second signals in which the second signal is a delayed first signal; and

an output formatter to receive the first and second signals and output the first and second signals at prescribed periods to produce the quadature component and the in-phase component of the digital signal.

2. (Currently Amended) The apparatus of claim 1, wherein said analog-to-digital converter further comprises:

a digital sampler to sample the intermediate frequency signal; and

a zero-order hold device to determine an amplitude of the sampled intermediate frequency signal[[;]],

~~a quantizer to convert the sampled intermediate frequency signal processed by the zero-order hold device to a digital signal;~~

wherein the latch circuit includes a plurality of latches to transmit the digital signal from the quantizer to a plurality of channels after a prescribed time delay~~; and~~, and

wherein the output formatter includes a plurality of output formatters to periodically output the latched digital signal transmitted to corresponding channels of the plurality of channels.

3. (Original) The apparatus of claim 2, wherein each of said plurality of output formatters comprises:

a plurality of negators to negate the latched digital signal and output a negated latched signal; and

a plurality of selectors one to one coupled to each of the plurality of negators to select and output one of the negated latched signal and an unprocessed latched digital signal.

4. (Original) The apparatus of claim 3, wherein the plurality of output formatters comprise first and second output formatters, and wherein the output of each output formatter is received by a low pass filter.

5. (Previously Presented) The apparatus of claim 2, wherein the plurality of channels comprise an In-phase channel and a Quadrature channel.

6. (Original) An analog-to-digital converter, comprising:

a digital sampler to sample an intermediate frequency signal;

a zero-order holder to determine an amplitude of the sampled intermediate frequency signal;

a quantizer to convert the sampled intermediate frequency signal processed by the zero-order holder to a digital signal;

a plurality of latches to transmit the digital signal to a plurality of channels after a prescribed time delay; and

a plurality of output formatters to periodically output the latched digital signal transmitted to corresponding channels of the plurality of channels.

7. (Original) The apparatus of claim 6, wherein each of said plurality of output formatters comprises:

a plurality of negators to negate the latched digital signal and output a negated latched signal; and

a plurality of selectors to select and output one of the negated latched signal and an unprocessed latched digital signal.

8. (Original) The apparatus of claim 7, wherein the plurality of output formatters comprise a first and second output formatter, and wherein the output of each output formatter is received by a low pass filter.

9. (Original) The apparatus of claim 6, wherein the plurality of channels comprise an I channel and a Q channel.

10. (Previously Presented) A signal processor, comprising:

a digitizer, which receives an analog signal and generates a digital signal, wherein the digitizer comprises:

a sampler, which receives and samples the analog signal,

a zero order hold circuit, which receives an output of the sampler and determines an amplitude of the received signal, and

a quantizer, which receives an output of the zero order hold circuit and generates the digital signal,

a channel separator, which receives the digital signal from the digitizer and separates the digital signal into at least 2 channels, each channel having a different phase; and

a phase shift controller, which receives a clock signal and controls the phase shifting of the channel separator.

11. (Original) The signal processor of claim 10, wherein the channels comprise a Q channel and an I channel having a phase difference of approximately 90□ .

12. (Original) The signal processor of claim 10, wherein the analog signal is an intermediate frequency CDMA formatted signal.

13. (Original) The signal processor of claim 12, wherein an output of the signal processor is a QPSK modulated digital signal, having a first component and a second component out of phase with the first component.

14. (Original) The signal processor of claim 10, wherein the channel separator comprises:

a latch circuit, which receives the digital signal and outputs a first signal and a second signal, wherein the second signal is a delayed first signal;

an output formatter, which receives the first and second signals and outputs the first and second signals at prescribed periods.

15. (Original) The signal processor of claim 14, wherein the latch circuit comprises a first latch, a second latch, and a third latch, wherein the output formatter comprises a first output formatter and a second output formatter, and wherein the first latch receives the digital signal from the digitizer, the second latch receives the output of the first latch and provides the first signal to the first output formatter and the third latch, and the third latch provides the second signal to the second output formatter.

16. (Original) The signal processor of claim 15, wherein the phase shift controller provides the clock signal to the first, second, and third latches to control the phase shifting, and provides a control signal to the first and second output formatters to control output periods.

17. (Original) The signal processor of claim 15, wherein the first and second output formatters each comprise:

a plurality of negators, which receive and negate the corresponding first or second signal; and

a plurality of selectors to select and output one of the negated signal from the negator and the corresponding first or second signal, wherein each one of the plurality of negators is coupled to one of the plurality of selectors.

18. (Canceled)

19. (Original) The signal processor of claim 10, wherein the phase shift controller comprises:

a plurality of buffers to receive and forward the clock signal; and

a logic circuit responsive to a buffered clock signal to generate a control signal to control an output of the channel separator.

20. (Original) The signal processor of claim 10, further comprising a plurality of Finite Impulse Response (FIR) filters coupled to receive an output of the channel separator, wherein an individual FIR filter is coupled to each channel of the at least two channels.

21. (Currently Amended) A demodulator for a CDMA receiver, comprising:

an input circuit to amplify a filtered CDMA formatted input signal;

a first signal processor to generate an intermediate frequency CDMA signal based on the amplified input signal; a second signal processor to output first and second digital signals on first and second channels, respectively, based on the intermediated frequency CDMA signal, said second signal processor having an analog-to-digital converter to convert the intermediate frequency CDMA signal to an intermediate digital signal and a channel separator to generate the first and second digital signals based on the intermediate digital signal; and

an output circuit to output a demodulated output signal based on the first and second digital signals, said output circuit having first and second Finite Impulse Response (FIR) filters to receive and filter the first and second digital signals, respectively, wherein the

first and second digital signals have different phases,

wherein the analog-to-digital converter device includes:

a quantizer to convert the intermediate frequency signal into the digital signal;

a latch circuit to receive the digital signal and output first and second signals in which the second signal is a delayed first signal; and

an output formatter to receive the first and second signals and output the first and second signals at prescribed periods to produce the quadature component and the in-phase component of the digital signal.

22. (Currently Amended) A method comprising:

converting an analog signal to a digital signal in an analog-to-digital converter; and

separating components of the digital signal from the digital signal in the analog-to-digital converter,

wherein separating the components of the digital signal uses at least one from:

at least one buffer;

at least one latch;

at least one flip-flop; and

at least one formatter.

23. (Previously Presented) The method of claim 22, wherein the components of the digital signal are:

an in-phase component of the digital signal; and

a quadrature component of the digital signal.

24. (Canceled).

25. (Previously Presented) The method of claim 22, wherein the analog signal embodies a CDMA communication signal.

26. (Previously Presented) The method of claim 23, wherein:

an in-phase component of the digital signal is associated with an in-phase component of the analog signal;

the quadrature component of the digital signal is associated with the quadrature component of the analog signal; and

the quadrature component of the analog signal is 90 degrees out of phase with the in-phase component of the analog signal.

27. (Previously Presented) The method of claim 22, wherein the converting the analog signal to the digital signal comprises:

sampling the analog signal to produce a sampled analog signal; and

quantizing the sampled analog signal to produce the digital signal.

28. (Previously Presented) The method of claim 27, wherein sampling the analog signal comprises sampling at a frequency that is four times the frequency of each component of the digital signal.

29. (Previously Presented) The method of claim 28, wherein the separating components of the digital signal from the digital signal comprises:

outputting on a first channel bits of the digital signal that are associated with the in-phase component of the digital signal; and

outputting on a second channel bits of the digital signal that are associated with the quadrature component of the digital signal.

30. (Previously Presented) The method of claim 29, wherein:

each bit of said bits of the digital signal that are associated with the in-phase component of the digital signal is separated by three consecutive bits that are not associated with the in-phase component of the digital signal;

each bit of said bits of the digital signal that are associated with the quadrature component of the digital signal is separated by three consecutive bits that are not associated with the quadrature component of the digital signal; and

each bit of said bits of the digital signal that are associated with the in-phase component of the digital signal are adjacent a bit of said of the digital signal that is associated with the quadrature component of the digital signal.

31. (Previously Presented) The method of claim 30, wherein each bit of said bits of the digital signal that are associated with the in-phase component of the digital signal are preceding a bit of said of the digital signal that is associated with the quadrature component of the digital signal.

32. (Currently Amended) An apparatus configured to:

convert an analog signal to a digital signal in an analog-to-digital converter; and

separate components of the digital signal from the digital signal in the analog-to-digital converter,

wherein for separating the components of the digital signal, the apparatus comprises at least one from:

at least one buffer;

at least one latch;

at least one flip-flop; and

at least one formatter.

33. (Previously Presented) The apparatus of claim 32, wherein the components of the digital signal are:

an in-phase component of the digital signal; and

a quadrature component of the digital signal.

34. (Canceled).

35. (Previously Presented) The apparatus of claim 32, wherein the analog signal embodies a CDMA communication signal.

36. (Previously Presented) The apparatus of claim 32, wherein:

an in-phase component of the digital signal is associated with an in-phase component of the analog signal;

the quadrature component of the digital signal is associated with the quadrature component of the analog signal; and

the quadrature component of the analog signal is 90 degrees out of phase with the in-phase component of the analog signal.

37. (Previously Presented) The apparatus of claim 32, wherein to convert the analog signal to the digital signal comprises:

sampling the analog signal to produce a sampled analog signal; and

quantizing the sampled analog signal to produce the digital signal.

38. (Previously Presented) The apparatus of claim 32, wherein to sample the analog signal comprises sampling at a frequency that is four times the frequency of each component of the digital signal.

39. (Previously Presented) The apparatus of claim 38, wherein to separate components of the digital signal from the digital signal comprises:

outputting on a first channel bits of the digital signal that are associated with the in-phase component of the digital signal; and

outputting on a second channel bits of the digital signal that are associated with the quadrature component of the digital signal.

40. (Previously Presented) The apparatus of claim 39, wherein:

each bit of said bits of the digital signal that are associated with the in-phase component of the digital signal is separated by three consecutive bits that are not associated with the in-phase component of the digital signal;

each bit of said bits of the digital signal that are associated with the quadrature component of the digital signal is separated by three consecutive bits that are not associated with the quadrature component of the digital signal; and

each bit of said bits of the digital signal that are associated with the in-phase component of the digital signal are adjacent a bit of said of the digital signal that is associated with the quadrature component of the digital signal.

41. (Previously Presented) The apparatus of claim 40, wherein each bit of said bits of the digital signal that are associated with the in-phase component of the digital signal are preceding a bit of said of the digital signal that is associated with the quadrature component of the digital signal.

42. (Currently Amended) An apparatus comprising:

an analog-to-digital converter;

a means for converting an analog signal to a digital signal in the analog-to-digital converter; and

a means for separating components of the digital signal from the digital signal in the analog-to-digital converter,

wherein the analog-to-digital converter device includes:

quantizer means for converting the intermediate frequency signal into the digital signal;

latch means for receiving the digital signal and output first and second signals in which the second signal is a delayed first signal; and

output formatter means for receiving the first and second signals and outputting the first and second signals at prescribed periods to produce the separating

components, which correspond to a quadature component and an in-phase component of the digital signal.